OIPE
APR 0 2 2001
PATENT & TRADEMARK OFFICE

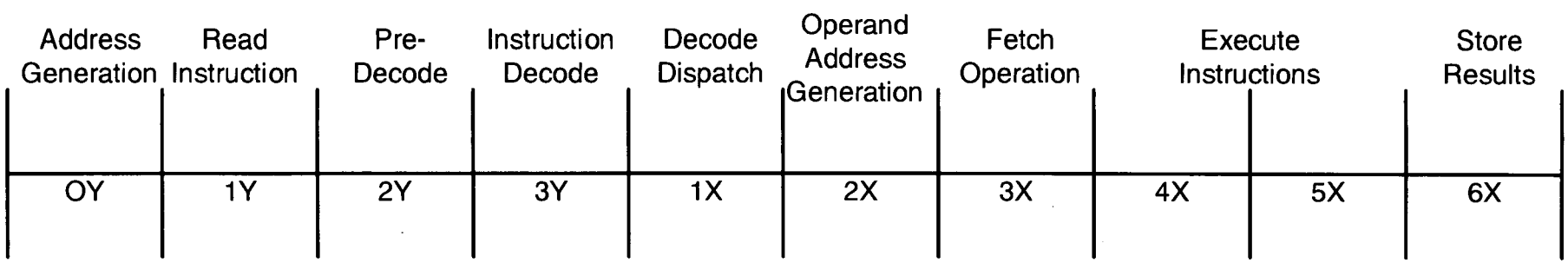


FIG. 1

PATENT & TRADEMARK OFFICE
APR 0 2 2001
OIPE
JC182

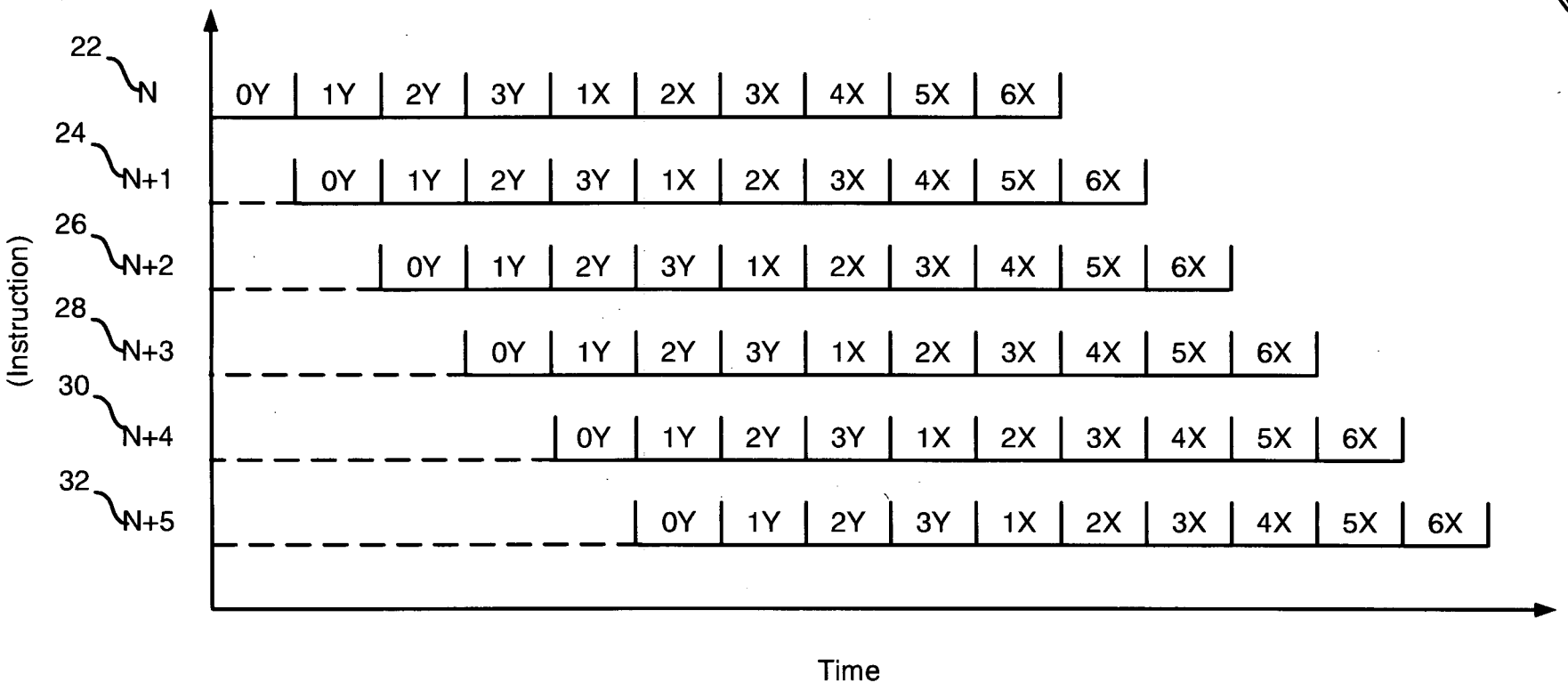


FIG. 2

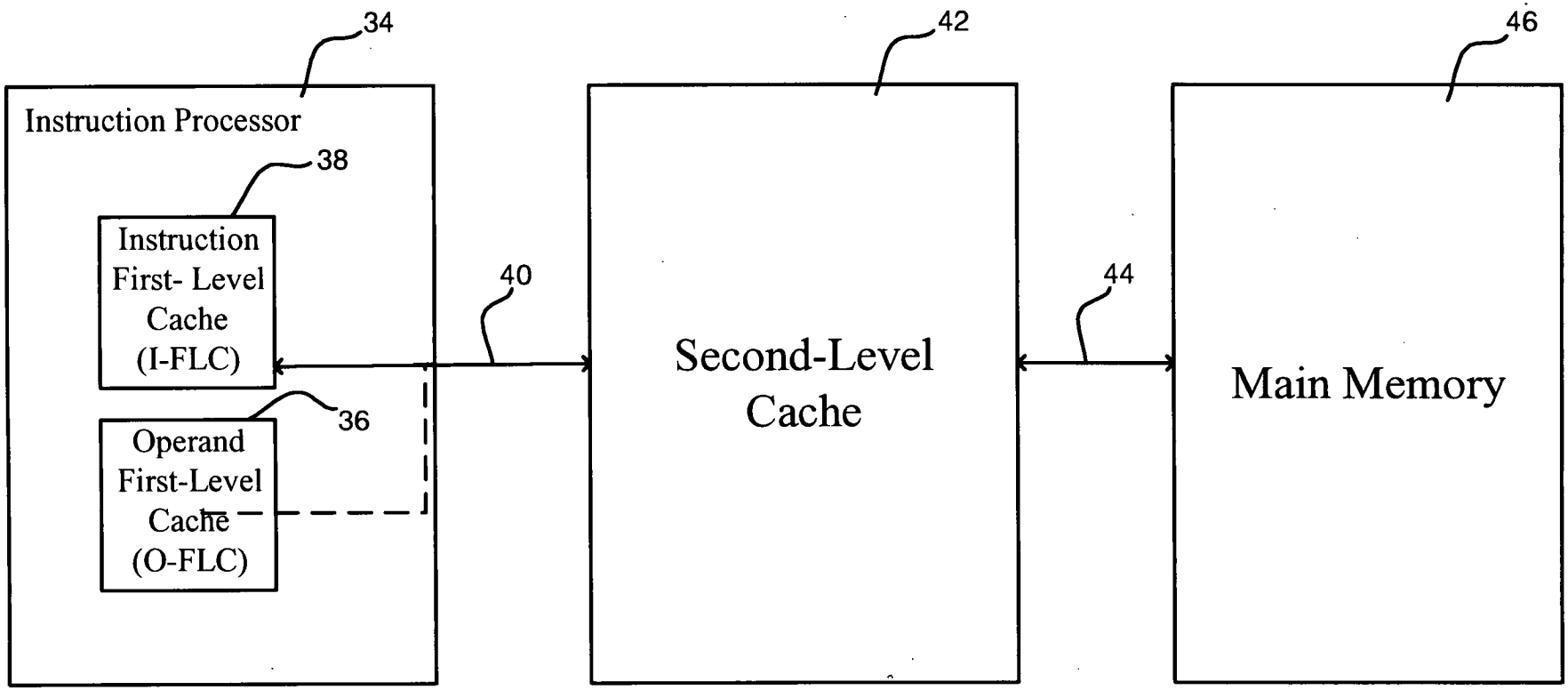

34
Instruction Processor
38
Instruction First- Level Cache (I-FLC)
36
Operand First-Level Cache (O-FLC)
40
42
Second-Level Cache
44
46
Main Memory

FIG. 3

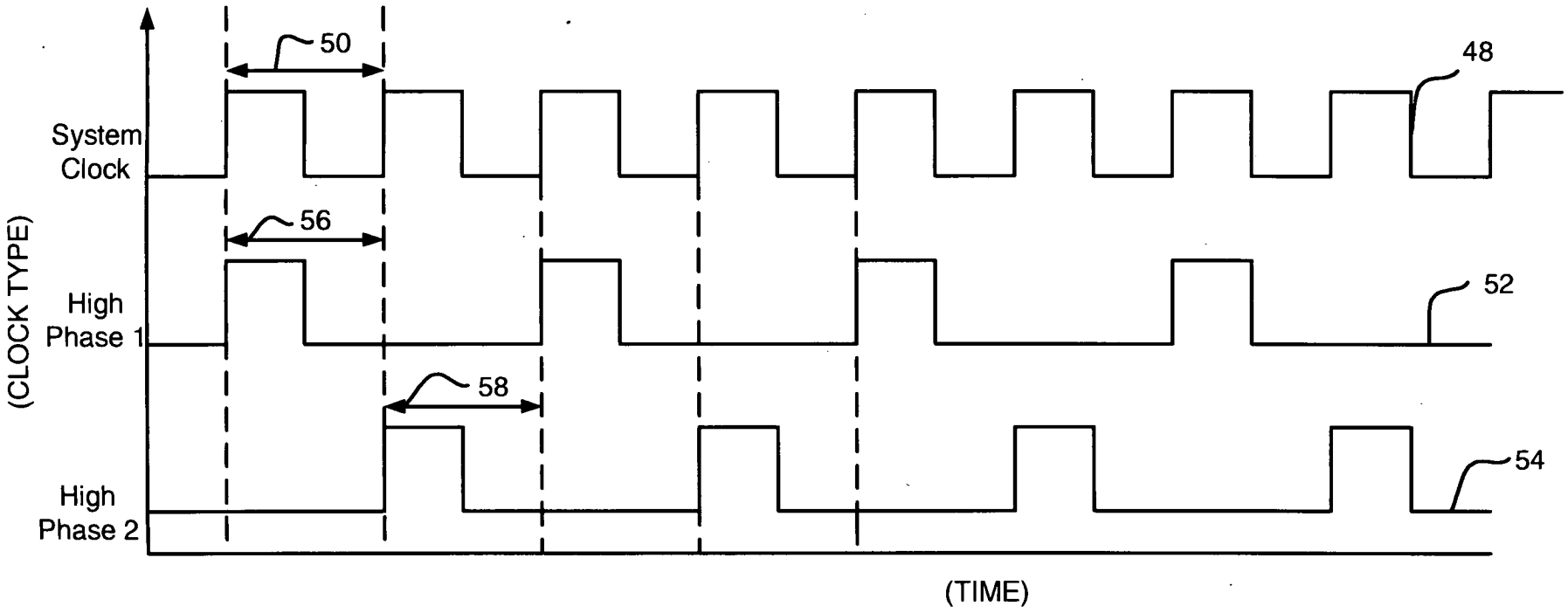

50
48
System
Clock
56
52
High
Phase 1
58
54
High
Phase 2
(CLOCK TYPE)
(TIME)

FIG. 4

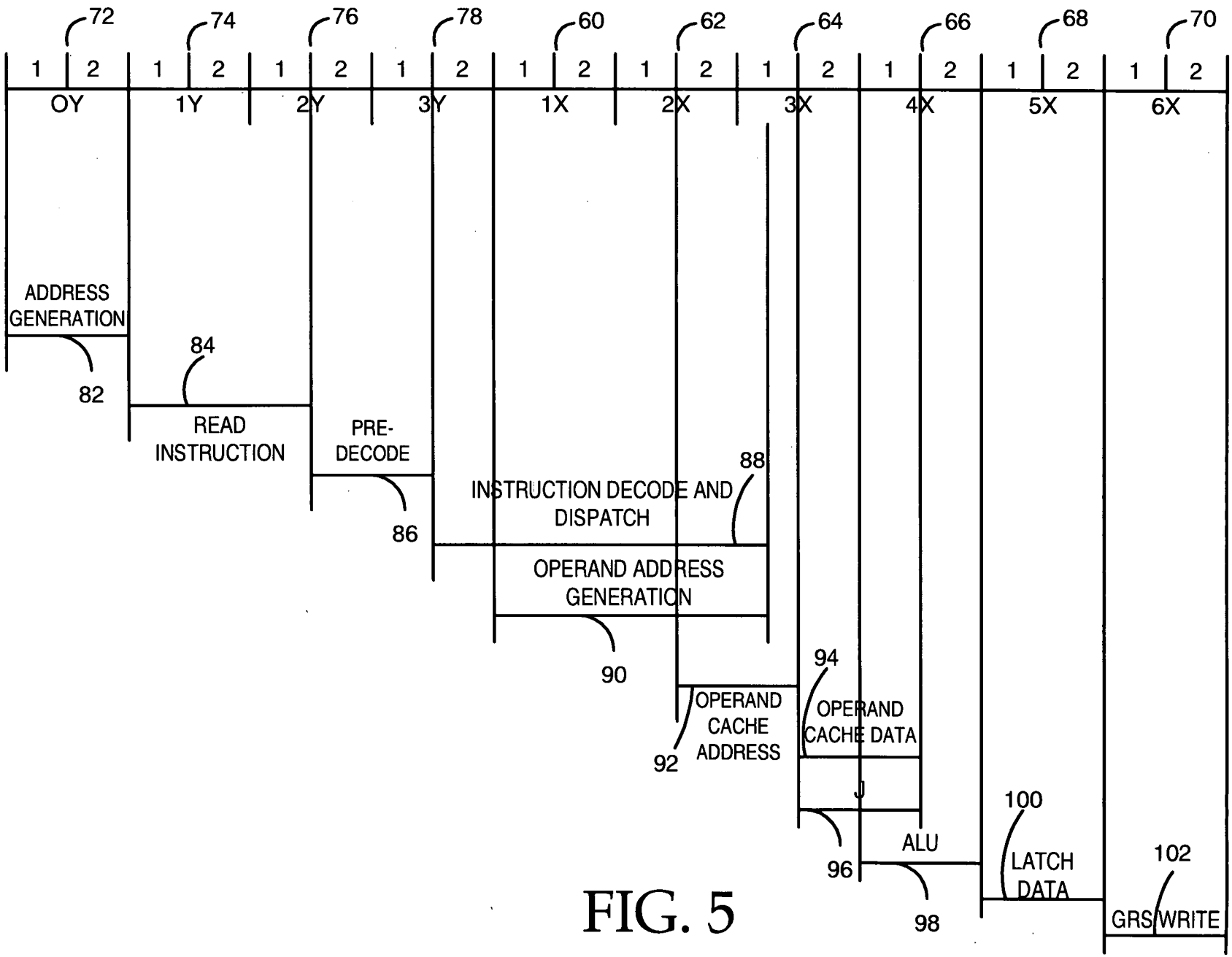

72
74
76
78
60
62
64
66
68
70
1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2
OY
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
ADDRESS GENERATION
82
84
READ INSTRUCTION
PRE-DECODE
86
88
INSTRUCTION DECODE AND DISPATCH
OPERAND ADDRESS GENERATION
90
92
OPERAND CACHE ADDRESS
94
OPERAND CACHE DATA
96
ALU
98
100
LATCH DATA
102
GRS WRITE

FIG. 5

TOSHIBA TMP92C060

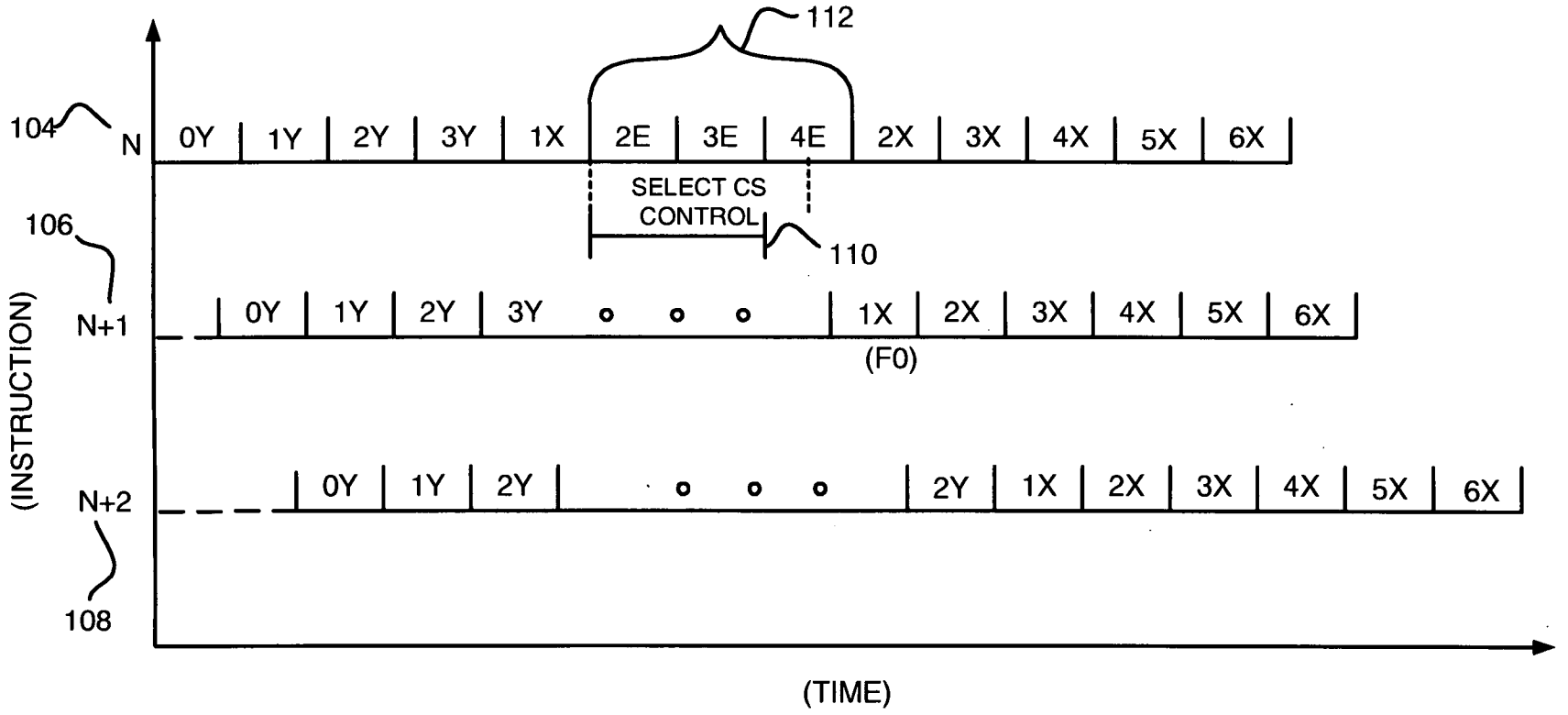


FIG. 6

TO2004 4h22250

FIG. 7

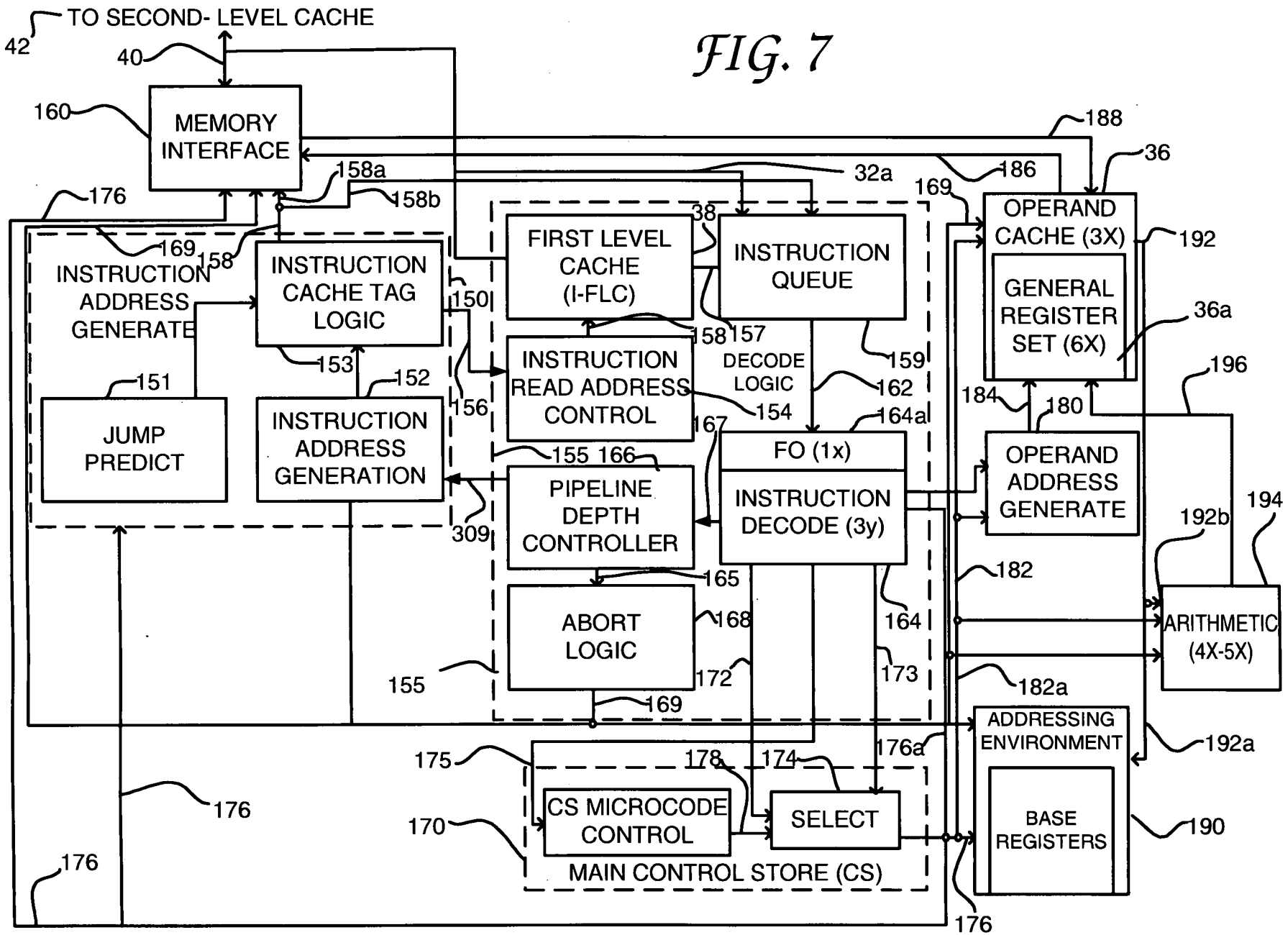
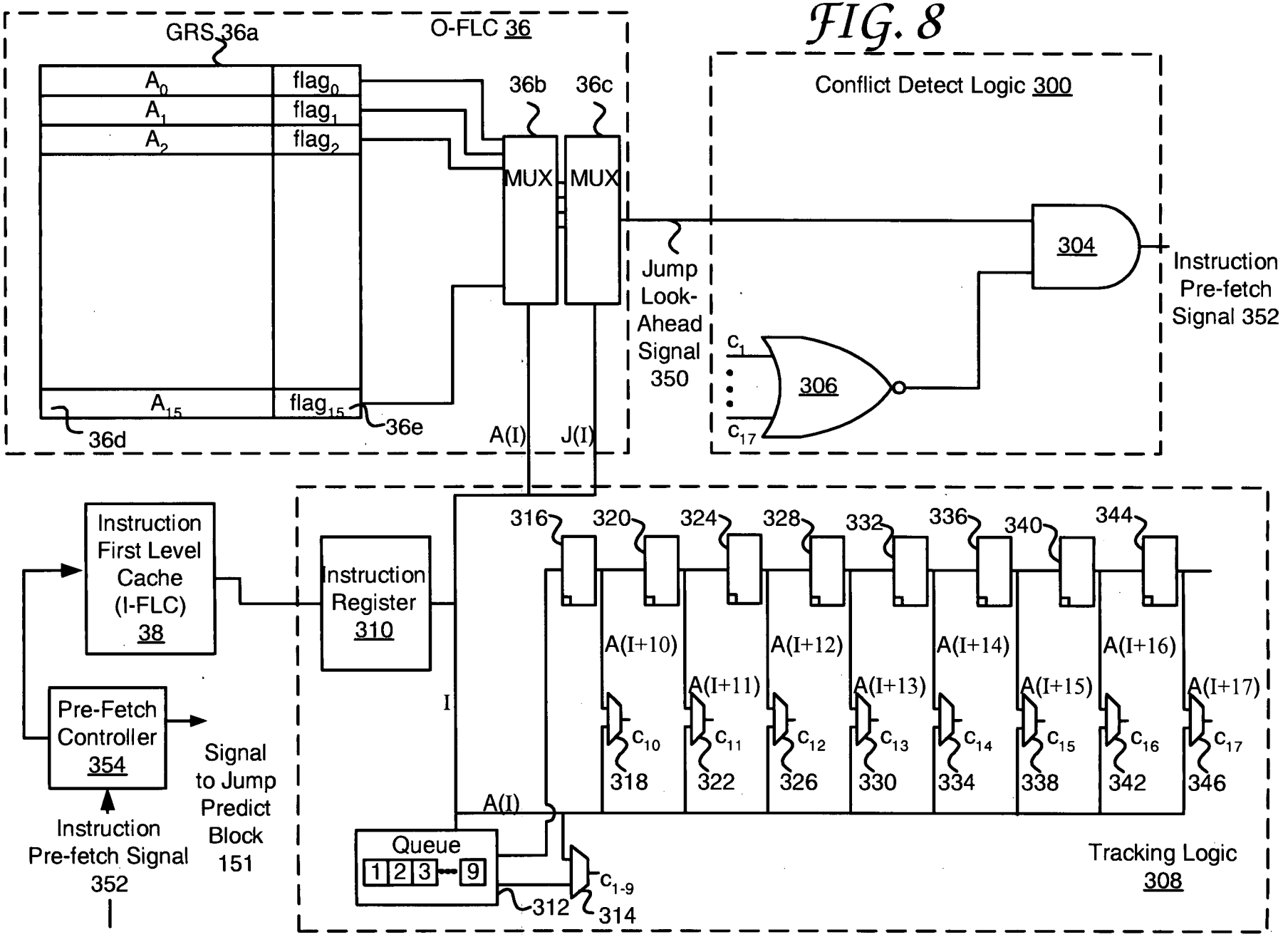


FIG. 8


GRS 36a
O-FLC 36
A0
A1
A2
A15
flag0
flag1
flag2
flag15
36b
36c
MUX
MUX
36d
36e
A(I)
J(I)
Conflict Detect Logic 300
304
306
c1
c17
Jump Look-Ahead Signal 350
Instruction Pre-fetch Signal 352
Instruction First Level Cache (I-FLC) 38
Instruction Register 310
Pre-Fetch Controller 354
Signal to Jump Predict Block 151
Instruction Pre-fetch Signal 352
I
316
320
324
328
332
336
340
344
A(I+10)
A(I+11)
A(I+12)
A(I+13)
A(I+14)
A(I+15)
A(I+16)
A(I+17)
c10
c11
c12
c13
c14
c15
c16
c17
318
322
326
330
334
338
342
346
A(I)
Queue
1 2 3 9
c1-9
312
314
Tracking Logic 308

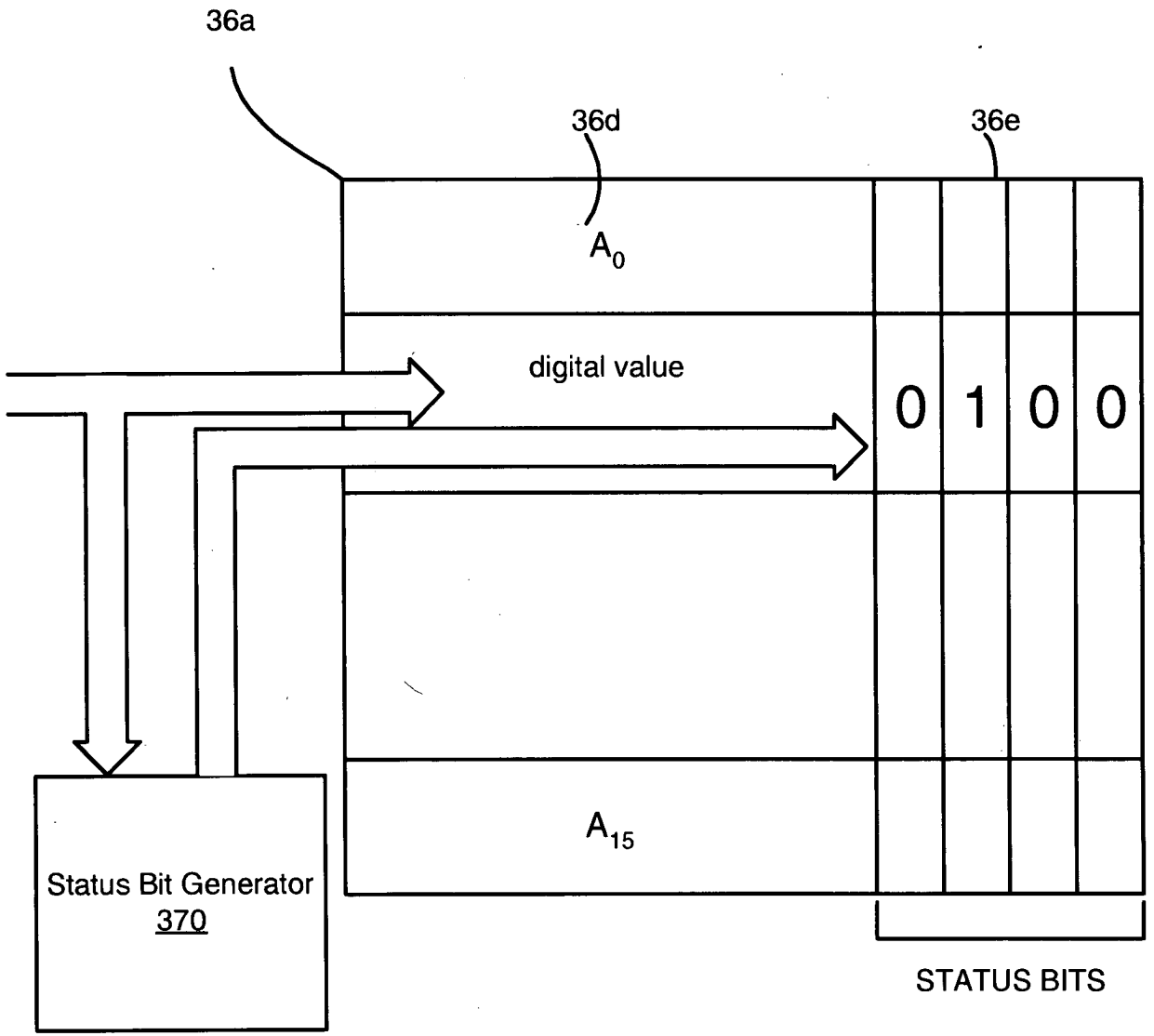

36a
36d
36e
A_0
digital value
0 1 0 0
A_{15}
Status Bit Generator
370
STATUS BITS

FIG. 9